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| EXAMINER | |
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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Paper No. 20

Application Number: 09/028,276
Filing Date: 02/24/98
Appellant(s): ATSUMI, SHIGERU



Joseph M. Potenza
For Appellant

**EXAMINER'S ANSWER**

This is in response to appellant's brief on appeal filed 08/17/00.

***(1) Real Party in Interest***

A statement identifying the real party in interest is contained in the brief.

*(2) Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

*(3) Status of Claims*

The statement of the status of the claims contained in the brief is correct.

*(4) Status of Amendments After Final*

No amendment after final has been filed.

*(5) Summary of Invention*

The summary of invention contained in the brief is correct.

*(6) Issues*

The appellant's statement of the issues in the brief is correct.

*(7) Grouping of Claims*

The rejection of claims 1-9, 13, 14 and 21-42 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

*(8) Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

*(9) Prior Art of Record*

| | | |
|---|---|---|
| 4,471,373 | Shimizu et al. | 9-1984 |

*(10) Grounds of Rejection*

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 102***

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 21-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimizu et al. (U.S. Patent No. 4,471,373).

In re claim 1 and 21-26, Shimizu (Figs. 1-3, 18) discloses a semiconductor integrated circuit device comprising a semiconductor substrate (10) on which a plurality of transistors (Q1, Q2, QE1, QE2, QE3) including gate insulation films of different thicknesses are formed; an input/output terminal (5) formed on the substrate, wherein a transistor (QE2) physically connected directly to the input/output terminal, absent any intervening elements, being one of the transistors other than a transistor having the thinnest gate insulation film.

In re claim 2, Shimizu discloses the device of claim 1, further comprising a power supply terminal (5), a transistor (QE3) connected directly to the power supply terminal being one of the transistors other than the transistor having the thinnest gate insulation film.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary

skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-9, 13-14 and 27-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (U.S. Patent No. 4,471,373).

In re claims 3-9, 13-14 and 27-42, Shimizu (Figs. 1-3, 18) discloses the devices of claims 1 and 24 respectively, including a memory array (2), a decoder portion (3), an input/output circuit (4), and enhancement type MIS transistors having a high breakdown voltage structure, i.e. a thick gate oxide film, and terminals for external connections (5) (column 1, lines 63-68; column 2, lines 23-63). Shimizu discloses the use of thin gate oxide transistors for the 'read' operation of an EPROM device and thick gate oxide transistors used for the 'write' operation, as well as other peripheral circuits (column 2, lines 45-51) Shimizu does not expressly disclose a ground terminal connected to the power supply terminal, a regulator circuit or a level shifter circuit of which one of the transistors receiving a lower level signal is a transistor having the thinnest gate insulation film. However, it would have been obvious to one skilled in the art at the time of the invention to couple a power supply line to a respective ground line. With the use of thin gate oxide transistors and lower voltages in the memory array and thick gate oxide transistors with higher voltages for peripheral circuits with a decoder circuit in between, it would have been obvious to one skilled in the art at the time of the invention to construct other in between circuits for the purpose of creating a buffer between the low and high voltage regions of the circuit.

*(11) Response to Argument*

Applicant argues on pp. 11 of the Appeal Brief that "Shimizu lacks a teaching or suggestion that the transistor QE2 is physically connected directly to the input/output terminal

(5), as called for in claim 1, and that the transistor QE2 is connected directly to the input/output terminal (5), absent any intervening elements, as called for in claim 21." Figures 1-3 of Shimizu clearly detail three regions of a memory circuit (Fig. 1) and the three types of transistors, A, B and C (Figs. 2 and 3) that correspond to each section of the circuit. Column 2, lines 40-45 explain that the transistor C, with the thickest gate oxide region is used for the high voltage peripheral circuit section. This region corresponds to the transistor QE3, column 7, lines 1-11). Upon close inspection of the passage (column 6, lines 66-68), one will see that what the appellant interprets as an aluminum wire connecting the input/output pad with the gate of the transistor, is actually the patterned gate itself. Thus, the transistor is demonstrated to be "physically connected directly" to the input/output terminal (5) and "absent any intervening elements."

In regards to the argument concerning claim 32, in which the appellant charges that the two regions are "always connected directly", the same argument applies. Appellant further argues in favor of the above claim language not being supported by the different thickness gate oxide transistors being used for different functions and thus not "always connected". However, appellant will note that the enhancement-type transistors referred to (column 7, lines 7-8) are the transistors with the *thinner* gate oxide film, not the *thicker* gate oxide film as claimed.

Claims 3, 5, 6, 33, 34, 36 and 37 depend from claims 1 and 32 mentioned above.

Applicant argues that the cited reference in regards to claims 2, 22, 23, 25 and 26 does not disclose a transistor other than one with a thinnest gate insulation film connected to a power supply terminal. Referring back to column 2, the reference discloses the thick gate insulation film transistor C connected to a high voltage (power supply) 25 V circuit.

Lastly, appellant argues that the reference does not adequately disclose input buffer, output buffer circuits and level shifter circuits as claimed in claims 7-9, 27-31 and 37-41. However, these circuits are secondary and broadly claimed in contrast to the narrow limitations of the transistors with thin and thick gate insulation films. Shimizu discloses a decoder circuit and an input/output circuit but does disclose the specific claimed limitations regarding thick gate insulation transistors on the peripheral edge of the integrated circuit. It would have been obvious to one skilled in the art at the time of the invention to substitute, for example, a level shifter for a decoder, for a flip-flop, as all these circuits are used for comparative logic and are standard internal devices in an integrated circuit.

Drawings: The objection to the drawings is withdrawn.

For the above reasons, it is believed that the rejections should be sustained.

An Appeal Conference was held with Acting SPE, Pimary Examiner Jerome Jackson on 12/29/00

Respectfully submitted,

Jesse A Fenty
Examiner
Art Unit 2815

JAF
December 29, 2000

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Concur w/ E's Jackson & Fenty

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